An 8-bit 120-MS/s Interleaved CMOS Pipeline ADC Based on MOS Parametric Amplification

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Abstract—This brief presents an 8-bit 120-MS/s time-interleaved pipeline analog-to-digital converter (ADC) fully based on MOS discrete-time parametric amplification. The ADC, fabricated in a 130-nm CMOS logic process, features an active area below 0.12 mm², where only MOS devices are used. Measurement results for a 20-MHz input signal shows that the ADC achieves 39.7 dB of signal-to-noise ratio, 49.3 dB of spurious-free dynamic range, and 14.12 MHz input signal, for a 20-MHz input signal shows that the ADC achieves 39.7 dB of signal-to-noise ratio, 49.3 dB of spurious-free dynamic range, and 1.2-V supply.

Index Terms—Analog-to-digital converter (ADC), MOS parametric amplification, pipeline, time-interleaved.

I. INTRODUCTION

Technology scaling is raising many issues for analog circuit design, such as intrinsic device gain, supply voltage, and device variability. In particular, for switched-capacitor (SC) realizations, performance degradation increases the difficulty to realize accurate charge transfers in the traditional manner, i.e., based on closed-loop operational amplifier (opamp) structures. Additionally, to reach a higher operation frequency, these opamps need a high gain–bandwidth product, reflecting an increase on power consumption. Different alternative solutions have recently been proposed, namely, open-loop amplification [1], comparator based [2], zero-crossing based [3], MOS discrete-time (DT) parametric amplification (MPA) [4], and dynamic source follower (SF) based [5]. With the exception of MPA, all of these techniques have already been applied to pipeline analog-to-digital converters (ADCs). However, their energy and area efficiency values are much dependent on the optimum resolution per stage, scaling of capacitance values, and residue amplifier topology for each multiplying digital-to-analog converter (MDAC) block.

Fig. 1. ADC architecture.

Silicon realizations using the DT MPA concept have already been demonstrated in a low-speed SC amplifier [4] and in a finite-impulse response low-pass filter circuit internally operating at a clock rate of 80 MHz [6]. Notice also that the technique proposed in [5] does not use any kind of MPA.

This brief describes a complete 8-bit time-interleaved pipeline ADC that uses the concept of MPA in all the analog blocks of the architecture. The simplicity of the basic and original MPA structure [4] is preserved, but to reach higher gains, one terminal of the MOS capacitor (MOSCAP) is floating. In addition, in contrast to other solutions that, in some way, include metal capacitor structures in their design, this ADC only uses MOS devices, and therefore, it is fully compatible with standard CMOS digital processes. Moreover, based on the authors’ knowledge, this work describes the first silicon proven high-speed pipeline ADC using the DT MPA concept.

This brief is organized as follows. In Section II, the adopted architecture is presented. In Section III, the DT MPA principle is revisited, and a circuit modification is proposed. In Section IV, each building block is presented, explicitly showing how the MPA technique has efficiently been applied. In Section V, a simplified ADC noise analysis model is described. Section VI shows the obtained experimental results, and finally, in Section VII, the conclusions are gathered.

II. ADC ARCHITECTURE

The two-channel interleaved ADC is shown in Fig. 1. Each channel operates at half of the conversion rate, i.e., \( F_S/2 \), and it comprises a sample-and-hold (S/H) followed by six pipelined stages with minimum resolution (1.5 bits) and by a 2-bit Flash quantizer (FQ). The 14 output bits are digitally synchronized, and 8 bits are available after digital correction. Pipeline stages consist of two types, namely, N and P. These two versions are needed to efficiently deal with different input and output common-mode (CM) voltages resulting from each...
type of stage, which affect the gain in the MPA structures. For example, N-type stages sample an input signal with a higher input CM voltage and produce a signal with a lower output CM voltage, i.e., $V_{CMO}$. P-type stages work in the opposite way. The stages process differential signals up to 400 mVpp.

### III. Modified MOS Parametric Amplifier

Small values of signal voltage amplification, e.g., to implement a multiply-by-two residue amplifier (MBTA), can be achieved by using the parametric MOS structure described in [4], where a DT amplifier is evaluated rather than a continuous-time configuration, as analyzed in [7]. In this amplifier, the gain is set through the reduction of the total equivalent gate capacitance of a single MOSCAP device while maintaining the total gate charge between the sampling phase $\phi_1$ and the amplification phase $\phi_2$. As explained in [4], the capacitance reduction of a MOSCAP can be achieved by moving it from inversion into depletion, as result of changing the control voltage $V_{control}$ applied to the drain from the negative power supply voltage $V_{SS}$ to the positive power supply $V_{DD}$, as shown in Fig. 2.

The first difference of the MOSCAP structure proposed in this work from the original structure used in [4] lies on the fact that two half-sized MOSCAPs are used in parallel rather than a single MOSCAP and with one of the tied terminals left floating. The division into more than two devices can be used for higher unit capacitance values. Care must be taken in not using either large $L$ (due to speed limitations) or minimum $L$ (due to short-length effects). As a consequence, with this modified structure, it becomes possible to decrease the effect of the extrinsic (overlap) gate capacitances during the amplification phase, i.e., $\phi_2$. Hence, amplification gains above 2 (considering the loading effect) can now be easier achieved with an nMOS-type MOSCAP (nMOSCAP). By properly adjusting the load, it becomes possible to design MBTA circuits with gain accuracy values above the 6-bit level, without a calibration scheme.

The amplifier gain shown in Fig. 3 was determined using the intrinsic MOS gate capacitance values obtained from electrical simulations of the circuit shown in Fig. 2. Fig. 3 also shows that the maximum achievable gain also depends on the CM level of the input voltage, reflecting how well the MOS device is biased in the inversion region during the sampling phase. Therefore, an appropriate dc level has to be carefully chosen.

### IV. MPA-Based ADC Design

Each pipelined stage uses the MPA technique, as shown in Fig. 4, in the 1.5-bit MDAC (following an open-loop approach) and in the comparators employed in the local 1.5-bit FQ.

#### A. Pipeline Stage of 1.5 bit

An N-type stage, as depicted in Fig. 5, has vertical symmetry, due to the interleaved operation. Each channel comprises a 1.5-bit FQ, a 1.5-bit MDAC composed of two half-MDACs (HMDACs) blocks, and two SFs. Both channels share the same replica bias circuit (RBC) to adjust the CM voltage $V_{CMO}$ of the stage, thus avoiding accumulation of dc errors through the pipeline chain and minimizing the impact of PVT variations. A similar configuration is used for the P-type stage.

#### B. RBC for Output CM Control

The RBC, as shown in Fig. 6, consists of four interleaved downscaled (by 2) HMDACs, for power and area savings, connected to a single (replica) SF circuit (downscaled by 2).
The input signal applied to the HMDAC block is amplified by the provided by the local FQ. Due to charge conservation, the cycle for charge redistribution by the loading, although it does not add any charge (differentially).

![Fig. 5. Block diagram of one interleaved pipelined stage (N-type).](image1)

The averaged voltage at the SF’s output is set and controlled by a feedback loop using a low-gain low-power operational transconductance amplifier (OTA; < 30 µW). The RBC provides the required regulated biasing voltage \( V_{BN} \) to the main SFs used in the output of each stage. The black filled areas of the voltage bars in Fig. 1 represent the allowed single-ended voltage levels at the different nodes, and the dashed line represents the \( V_{CMO} \) variations between stages. The \( V_{CMO} \) of an N-type stage is set to a lower value \( \left( V_{CMON} \approx 0.35 \, \text{V} \right) \) to properly drive the next P-type stage. Likewise, the \( V_{CMO} \) of a P-type stage is set to a higher value \( \left( V_{CMOP} \approx 0.75 \, \text{V} \right) \) to drive the next N-type stage. The OTA does not need a high bandwidth since it is not inserted in the main signal path. It can be designed with minimum current.

C. HMDAC Circuit

The schematic of an N-type HMDAC circuit [8] for the positive signal path is shown in Fig. 7. For the P-type version, the nMOSCAP and the pMOSCAP are interchanged. Moreover, the only difference between the positive and negative signals (either in the N- or P-type stage) is that signals \( X \) and \( Z \) from the local FQ are exchanged between the two HMDACs. MOSCAPs \( C_X \), \( C_Y \), and \( C_Z \), operating in the inversion region, perform the DAC function. \( C_Y \) is required to provide the same loading, although it does not add any charge (differentially).

Only one of these capacitors is selected in each clock cycle for charge redistribution by the \( X \), \( Y \), and \( Z \) codes provided by the local FQ. Due to charge conservation, the input signal applied to the HMDAC block is amplified by the

![Fig. 6. RBC (N-type).](image2)

The averaged voltage at the SF’s output is set and controlled by a feedback loop using a low-gain low-power operational transconductance amplifier (OTA; < 30 µW). The RBC provides the required regulated biasing voltage \( V_{BN} \) to the main SFs used in the output of each stage. The black filled areas of the voltage bars in Fig. 1 represent the allowed single-ended voltage levels at the different nodes, and the dashed line represents the \( V_{CMO} \) variations between stages. The \( V_{CMO} \) of an N-type stage is set to a lower value \( \left( V_{CMON} \approx 0.35 \, \text{V} \right) \) to properly drive the next P-type stage. Likewise, the \( V_{CMO} \) of a P-type stage is set to a higher value \( \left( V_{CMOP} \approx 0.75 \, \text{V} \right) \) to drive the next N-type stage. The OTA does not need a high bandwidth since it is not inserted in the main signal path. It can be designed with minimum current.

D. FQs of 1.5 bits

Each 1.5-bit FQ comprises two comparators, two digital latches, and an output encoder to provide the \( X \), \( Y \), and \( Z \) signals and the output bits. Each comparator consists of an input SC network that defines the desired threshold levels of \( \pm V_{REFD} / 4 \), followed by a positive-feedback latch (PFDL). As proposed in [9], to improve performance and reduce power, preamplification is embedded in the input SC network also by employing the MPA principle, as shown in Fig. 8. The circuit operates with two nonoverlapping phases, and each capacitor is implemented by means of a parametric MOSCAP, as described in Fig. 2. A detailed analysis is given in [9].

The threshold level does not directly depend on the load capacitance and can be adjusted by the ratio of \( C_1 \) and \( C_2 \) during \( \phi_1 \). The load capacitance \( C_1 \) only affects the circuit gain. The complete comparator schematic is shown in Fig. 9.
V. Noise Analysis

The pipeline structure of the ADC dictates that the noise budget for each MDAC stage has to be weighted by the total gain of precedent stages when referred to the converter’s input. Although MPA is intrinsically noiseless, the different $kT/C$ components (where $k$ is the Boltzmann’s constant, and $T$ is the absolute temperature) have to be taken into account. Additionally, other noise sources increase the total noise power at the SFs’ outputs during the amplification phase, including substrate noise and noise from the active devices used in the SF circuits [4].

Since the digital noise-coupling contribution through the substrate can be reduced by using well-known layout techniques, it can be neglected in this analysis. The total ADC noise performance is mostly dependent on the front-end S/H and on the first and second 1.5-bit MDACs. Hence, a simplified MDAC noise model, as shown in Fig. 10, can be used for noise analysis since the S/H can be treated as an MDAC in the $Y$ configuration.

The input-referred noise of each MDAC can be described by

$$\nu_{i,n,\text{MDAC}}^2 = 2 \cdot \left[ \frac{kT}{C_1} + \frac{kT}{C_2} + \frac{kT}{C_Y} \cdot \left( G_{\text{MPA},C} \right)^2 \right] + 2 \cdot \left[ \left( \frac{kT \cdot \gamma \cdot E_{\text{SF}}}{C_L} \right) \cdot \left( \frac{1}{G_{\text{MPA},C} \cdot G_{\text{SF}}} \right)^2 \right].$$

The first term represents the different $kT/C$ noise contributions related to the parametric and constant MOS capacitances (biased in the inversion region), and $G_{\text{MPA}}$ represents the intrinsic noiseless gain of the parametric structure [4]. The remaining terms describe the noise from the SF at the output node, which has to be input referred. $E_{\text{SF}}$ is the gain of the SF, which is slightly lower than unity mainly due to the body effect, $E_{\text{SF}}$ is the SF excess thermal noise factor ($E_{\text{SF}} \approx 2$), and $\gamma$ is the transistor’s excess noise factor ($\gamma \approx 1$). Since each stage is connected in a differential schematic, a factor of 2 is also affecting (2).

Considering that all MDACs have a similar input-referred noise level, the overall ADC input noise power is given by

$$\nu_{i,n,\text{ADC}}^2 = \frac{\nu_{i,n,\text{MDAC}}^2}{4^j}.$$ (3)

Additional noise components, such as quantization noise, RMS jitter noise, and differential nonlinearity (DNL) “grass” noise, increase the total input-referred noise power of the ADC. For an 8-bit ADC and considering a full-scale input signal, a noise power term due to 2-ps RMS jitter (corresponding to a 35.5-$\mu$VRMS noise voltage) and a DNL “grass” at 1/3 least significant bit (LSB) level (corresponding to 230 $\mu$VRMS), the expected SNR is about 40.5 dB (assuming $C_1 = 312 \text{ fF}$, $C_2 = 51 \text{ fF}$, $C_Y = 25 \text{ fF}$, and $C_L = 0.5 \text{ pF}$).

VI. Implementation and Measurement Results

An ADC prototype IC (micrograph shown in Fig. 11) was fabricated in a 130-nm 1P 8M CMOS pure logic process. To reduce mismatch effects, all MPA units in a stage of both channels have been laid out together using a common-centroid approach complemented by intensive postlayout simulations.

The ADC features an active area below 0.12 mm$^2$ and dissipates less than 14 mW at 120 MS/s and a 1.2-V supply. This total power, which excludes the external band-gap references, is distributed through digital correction (29%), the MPA cells and SFs (34%), and the comparator’s PFDL and clock buffers (37%). Notice that this ADC was not power optimized since all stages are equally sized to minimize layout effort. Since the SNR of a pipeline ADC is mainly determined by the front-end S/H, first and second stages [10], by downscaling the others, a power savings up to 50% could be reached in each MPA unit. From [11], the power-and-area figure-of-merit can be calculated with $\text{FOM} = P \cdot A / (2^{\text{ENOB}} \cdot F_S)$, where $P$ and $A$ are the total power and...
sweeping the input signal frequency at $F_s = 120$ MS/s, as shown in Fig. 14(a), and by sweeping the sampling rate for $f_{in} = 20$ MHz, as shown in Fig. 14(b). For $F_s = 120$ Hz, the ADC exhibits a flat ENOB higher than 6 bits (with a peak of 6.2 bits) up to $f_{in} = 41$ MHz [Fig. 14(a)]. The same flatness behavior in the ENOB is achieved for sampling rates up to 130 MS/s [Fig. 14(b)]. The ENOB variation between channels ranges from 0.1 bit for the best sample to 0.4 bit for the worst sample. Key features and measurement results are summarized in Table I.

VII. CONCLUSION

This brief has presented a MOS only 8-bit 120-MS/s interleaved pipeline ADC that extensively uses DT MPA. Measurements for a 20-MHz input signal shows that the ADC achieved, without calibration, 39.7 dB of SNR, 49.3 dB of SFDR, −47.5 dB of THD, 39.1 dB of SNDR, and 6.2 bits of ENOB.

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REFERENCES


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<tr>
<th>TABLE I</th>
<th>KEY FEATURES AND MEASURED RESULTS</th>
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<tbody>
<tr>
<td>Technology</td>
<td>CMOS 130 nm 1P 8M</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Resolution, Sampling Rate ($F_s$)</td>
<td>8-bit, 120 MS/s</td>
</tr>
<tr>
<td>Input full-scale (differential)</td>
<td>200 mVpp</td>
</tr>
<tr>
<td>Internal signal swing (differential)</td>
<td>400 mVpp</td>
</tr>
<tr>
<td>Power Consumption, Die Area</td>
<td>14 mW, 0.12 mm²</td>
</tr>
<tr>
<td>DNL ± INL</td>
<td>−0.8/+1.4 ; ±2.0/±2.0 1LSB/8bit</td>
</tr>
<tr>
<td>Meas. @ $F_s$=120 MS/s , @ $f_{in}$=20 MHz , @-0.055 dBFS</td>
<td></td>
</tr>
<tr>
<td>SNR, SFDR</td>
<td>39.7 dB, 49.3 dB</td>
</tr>
<tr>
<td>THD, SNDR</td>
<td>−47.5 dB, 39.1 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>6.2 bits</td>
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area, respectively. A FOM better than 191 fJ * mm²/conversion was achieved with this ADC. All capacitors are implemented only using MOS devices. Fig. 12 shows that the measured DNL and integral nonlinearity (INL) errors at 120 MS/s are within −0.8/+1.4 LSB and ±2.0 LSB, respectively. Fig. 13 displays a measured fast Fourier transform (FFT) for a 21-MHz input signal frequency $f_{in}$ and a 120-MS/s sampling frequency $F_s$. The circuit achieves a peak SNR of 39.7 dB, a spurious-free dynamic range (SFDR) of 49.3 dB, and a peak total harmonic distortion (THD) of −47.5 dB, corresponding to an effective number of bits (ENOB) of 6.2 bits. The dynamic performance of this ADC was experimentally evaluated in three different samples (mounted using direct bonding) by